**POORNIMA UNIVERSITY, JAIPUR**

**END SEMESTER EXAMINATION, April 2023**

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|  | **4BC2102** | Roll No. | Total Printed Pages: **2** |
| **4BC2102** |  |
| BCA II Year IV Semester (Back) End Semester Examination, April 2023  **(AIPA)** | |
| **BAP04102: Digital Electronics** | | | |

# Max. Time: **3**Hours. Max. Marks: **60**

Min. Passing Marks: **21**

Attempt **five** questions selecting one question from each Unit. There is internal choice from Unit I to Unit V. Marks of each question or its parts are indicated against each question / parts. Draw neat sketches wherever necessary to illustrate the answer. Assume missing data suitably (if any) and clearly indicate the same in the answer.

Use of following supporting material is permitted during examination for this subject.

# **1.----------------------------------------------** **2.-----------------------------------------**

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|  |  | **UNIT-I (CO1)** | **Marks** | **Bloom Level** |
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| **Q.1** | **(a)** | Convert the following decimal numbers to the indicated base:  (i) 7662.45 to octal.  (ii) 1838.257 to hexadecimal.  (iii) 174.174 to binary | **(6)** | **Evaluating** |
|  |  |  |  |  |
|  | **(b)** | Write about Alpha numeric code also mention its related two codes and the relation of alpha numeric codes with American Standard Code for Information Interchange and Extended Binary Coded Decimal Interchange Code. | **(6)** | **Analyzing** |
|  |  | **OR** |  |  |
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| **Q.2** | **(a)** | How errors may get introduced? Explain using error detecting and correcting codes with its two examples. | **(6)** | **creating** |
|  |  |  |  |  |
|  | **(b)** | Logic gate is a digital circuit, justify this statement by elaborating the meaning of logic also with another name of logic gates also the relation of these gates with Boolean expression. List the different types of logic gates with its truth table and Boolean expression. | **(6)** | **Analyzing** |
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|  |  | **UNIT-II (CO2)** |  |  |
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| **Q.3** | **(a)** | Why PMOS is not used in new designs? Mention and explain the other two logic families of MOSFET. | **(6)** | **creating** |
|  |  |  |  |  |
|  | **(b)** | Why “Schottkey transistor is used instead of normal transistors also elaborate concept of cut-off region, saturation etc. with the related sketch of Schottkey transistor and its symbol? | **(6)** | **Analyzing** |
|  |  |  |  |  |
|  |  | **OR** |  |  |
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| **Q.4** | **(a)** | Explain Tri-state logic, mentioning all three with its related sketches. | **(6)** | **creating** |
|  |  |  |  |  |
|  | **(b)** | Elaborate the relation of logic family with a set of compatible IC’s with the same logic levels and same supply voltages. Classify it on the basis of fabrication technology with in detail about” Bipolar logic families”. | **(6)** | **Analyzing** |
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|  |  | **UNIT-III (CO3)** |  |  |
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| **Q.5** | **(a)** | Design the logic diagram of full adder with sum (s) values(0,1,1,0,1,0,0,1) and Carry(C out) values(0,0,0,1,0,1,1,1) | **(6)** | **Evaluating** |
|  |  |  |  |  |
|  | **(b)** | Elaborate briefly with a sketch “Decoder”. | **(6)** | **creating** |
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|  |  | **OR** |  |  |
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| **Q.6** | **(a)** | Design the logic diagram of half subtractor with difference (D) values(0,1,1,0,1,0,0,1) and borrow(C) values(0,1,1,1,0,0,0,1) | **(6)** | **Evaluating** |
|  |  |  |  |  |
|  | **(b)** | Explain briefly the term “Encoder”. | **(6)** | **creating** |
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|  |  | **UNIT-IV (CO4)** |  |  |
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| **Q.7** | **(a)** | How a flip flop with 1-bit memory cell storing 1-bit of digital data is related with shift registers ?On the basis of the way the data is entered and retrieve ,mention and explain its classifications. | **(6)** | **Evaluating** |
|  |  |  |  |  |
|  | **(b)** | Analysis & design of synchronous sequential circuits, explain. | **(6)** | **creating** |
|  |  |  |  |  |
|  |  | **OR** |  |  |
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| **Q.8** | **(a)** | Design and explain a 3-bit Synchronous Counter. | **(6)** | **Analyzing** |
|  |  |  |  |  |
|  | **(b)** | Design a 4-bit Johnson Counter, mentioning the data shifting and its related waveforms and also the relation of serial input serial output shift register with Johnson counter. | **(6)** | **creating** |
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|  |  | **UNITV (CO5)** |  |  |
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| **Q.9** | **(a)** | What is PAL and PLA, explain briefly. | **(6)** | **creating** |
|  |  |  |  |  |
|  | **(b)** | Read and Write is the main memory of a digital system, justify this statement in detail with RAM classifications with its cell arrangement | **(6)** | **Analyzing** |
|  |  |  |  |  |
|  |  | **OR** |  |  |
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| **Q.10** | **(a)** | How the designing of digital systems are with flip flops and gates and the importance of including external flip flops in sequential programmable devices, explain? | **(6)** | **creating** |
|  |  |  |  |  |
|  | **(b)** | PROM cannot be reprogrammed, justify this statement with an appropriate example. | **(6)** | **Analyzing** |